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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/825,351	04/15/2004	Lindsey H. Hall	TI-35168	8635

23494 7590 12/23/2005

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EXAMINER
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FULK, STEVEN J

ART UNIT	PAPER NUMBER
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2891

DATE MAILED: 12/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)	
	10/825,351	HALL ET AL.	
	Examiner	Art Unit	
	Steven J. Fulk	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 28 October 2005.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) 11-15 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-10 and 16-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 July 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)             | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                                    |

**DETAILED ACTION**

***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-3, 9-10, 16 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagano et al. '327 in view of Gonzalez et al. '731.

Nagano et al. discloses a method of fabricating an integrated circuit and a method of reducing recess relief within an interconnect structure located in a layer of a semiconductor device comprising forming transistors on a semiconductor substrate, depositing dielectric layers over the transistors, forming an interconnect structure located in the dielectric layer, and forming a metal-insulator-metal capacitor on the interconnect structure (col. 3, lines 36-50). The reference further discloses the method to include conducting a fabrication process on the interconnect that recesses the interconnect and forms a recessed dielectric layer (col. 6, lines 46-67), and subsequently conducting a recess reduction etch to remove a portion of the recessed dielectric layer to reduce a relief of the recessed dielectric layer and form a substantially planar surface about the interconnect structure prior to forming the metal-insulator-metal capacitor (col. 7, lines 3-18). The references also discloses the recess reduction etch being performed under non-

oxidizing conditions (col. 7, lines 9-15), and the etch resulting in a recess depth of zero nanometers (col. 10, lines 9-13).

Nagano et al. does not explicitly disclose performing a post-planarization clean. Gonzalez et al. teaches a method of forming an interconnect by planarizing a layer of conductive material located within an opening over a dielectric layer (fig. 4-5), the planarizing leaving a residue on the surface of the dielectric (col. 5, lines 63-67), and performing a post-planarization clean to remove the residue and form a recessed interconnect and substrate (fig. 6-7, col. 5, lines 7-67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the post-planarization clean of Gonzalez et al. in the method of forming an interconnect of Nagano et al. One would have been motivated to do this because performing a post-planarization clean was a conventional method of removing residue left from a CMP step from the surface of a layer to prevent latent defects in the integrated circuit and improve device performance (Gonzalez et al., col. 5, lines 63-67).

3. Claims 4, 6-7, 17 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagano et al. '327 in view of Gonzalez et al. '731 as described above, and further in view of Dubin et al. '190.

Nagano et al. in view of Gonzalez et al. teaches all of the elements of claims 1 and 16, and also teaches the use of an argon gas dry etch to perform the recess reduction etch (Nagano et al., col. 7, lines 3-5). Nagano et al. in view of Gonzalez et al. teaches does not teach the dry etch gas mixture of the fluorinated hydrocarbon compound  $\text{CH}_2\text{F}_2$ , nitrogen or hydrogen, and argon gas. Dubin et al.

teaches the use of CH<sub>2</sub>F<sub>2</sub>, argon, and nitrogen to etch dielectric layers in the formation of an interconnect (¶18).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the etch gas mixture of Dubin et al. in the interconnect process of Nagano et al. in view of Gonzalez et al. because the mixture of fluorinated hydrocarbons, nitrogen, and argon is functionally equivalent for dielectric etching, and the mixture can be tailored to the etch rates of various dielectric materials.

4. Claims 5, 8, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagano et al. in view of Gonzalez et al. and Dubin et al. as described above, and further in view of Chen '003.

Nagano et al. in view of Gonzalez et al. teaches all of the elements of claims 1 and 16, but fails to teach the use of a fluorinated hydrocarbon flowing at about 20 sccm, argon flowing at about 100 sccm, and nitrogen or hydrogen flowing at about 100 sccm. Nagano et al. in view of Gonzalez et al. also fails to disclose the etch duration time. Chen teaches a method of forming an interconnect and metal-insulator-metal capacitor that uses a fluorinated hydrocarbon at a flow rate of about 20 sccm and uses inert gases at of flow of about 100 sccm (col. 9, lines 12-16). The reference also discloses performing a dielectric layer etch for about 10 seconds (col. 9, lines 3-7).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the claimed etch flow rates and etch time in the method of Nagano et al. in view of Gonzalez et al. because Chen teaches that the use of

these flow rates and etch time for this application was known, and evidence that the selection of the specified flow rates and etch time would have merely constituted an obvious optimization determinable through routine experimentation in order to tailor the dielectric etch to the desired etch rate and dielectric layer profile.

***Response to Arguments***

5. Applicant's arguments, see page 7, section I, filed October 28, 2005, with respect to the rejection of claim 5 under U.S.C. § 112 have been fully considered and are persuasive. The rejection of claim 5 under U.S.C. § 112 has been withdrawn.

6. Applicant's arguments with respect to claims 1-3, 9-10, 16 and 20 have been considered but are moot in view of the new ground(s) of rejection. Applicant amended the independent claims to include a post-planarization etch, which was not disclosed by Nagano et al. However, the new grounds of rejection based on Nagano et al. in view of Gonzalez et al. teaches all of the elements of the claims.

7. Applicant's arguments with respect to claims 4, 6-7, 17 and 19 have been considered but are moot in view of the new ground(s) of rejection. Applicant acknowledged that Dubin was offered to address the process conditions that might be used to remove a recess, and argued that Dubin did not disclose removing a portion of residue using a post-planarization clean. Examiner agrees that Dubin does not teach a post-planarization clean, however this argument is moot because the new grounds of rejection based on Nagano et al. in view of Gonzalez et al. and further in view of Dubin teaches all of the elements of the claims.

8. Applicant's arguments with respect to claims 5, 8 and 18 have been considered but are moot in view of the new ground(s) of rejection. Applicant acknowledged that Chen was offered to address the process conditions that might be used to remove a recess, and argued that Chen did not disclose removing a portion of residue using a post-planarization clean. Examiner agrees that Chen does not teach a post-planarization clean, however this argument is moot because the new grounds of rejection based on Nagano et al. in view of Gonzalez et al. and Dubin, and further in view of Chen teaches all of the elements of the claims.

***Conclusion***

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven J. Fulk whose telephone number is (571) 272-8323. The examiner can normally be reached on Monday through Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571) 272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sjf  
12/19/05

A handwritten signature in black ink, appearing to read 'Bradley K. Smith', written in a cursive style.

**BRADLEY K. SMITH**  
**PRIMARY EXAMINER**